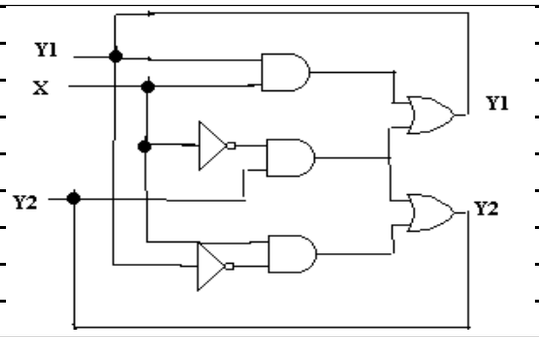
	Department of Electrical and Electronics Engineering
	DIGITAL LOGIC CIRCUITS-UBEE303
	UNIT-I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES
	PART-A
1	How many bits are required to represent the decimal numbers in the range 0 to 999 using straightbinary codes and using BCD codes? How is the letter A coded in the ASCII code?
2	Show that the excess-3code is self-complementing. Complementing property:
3	Determine $(377)_{10}$ in Octal and Hexa-decimal equivalent
4	What is meant by weighted and non-weightedcode?
5	Add the decimals 67and 78 using excess-3 code.
6	Add the decimals 57and 68 using 8421BCDcode.
7	Write the two properties ofGray code &mentionthe application ofGraycode Properties:
8	Give the classification of logic families
9	Conver tthe following hexadecimalnumbers into decimalnumbers: 263,1C3
10	Which gates are called as the universal gates? What are its advantages?
11	(a)Convert$(11001010)_2$ into graycode (b)(11101101) gray codeintobinary code.
12	Mention the important characteristics of digital IC's?
13	Define Fan in and Fan-out?
14	Define power dissipation and noise margin?
15	What is propagation delay?
16	What are the types of TTL logic?
17	What is depletion mode and enhancement mode operation MOS?
18	Mention the characteristics of MOS transistor?
19	State advantages and disadvantages of TTL
20	What is hamming code?
21	Compare the totem pole output with open collector output.
22	What is the advantages of ECL over TTL?
	PART- B
1	Compare the general characteristics of TTL, ECL and CMOS logic families.
2	Explain about various TTL parameters in detail
3	Explain the working of (i)CMOSNAND and NOR gate,(ii) ECL AND gate.
4	Explain in detail about the classification of Binary codes
5	i) State the differences between 1's complement and 2's complement ii) Determine the hamming code for the data 1011using even parity. Subtraction with suitable examples.
6	Given that a frame with bit sequence 1101011011 is transmitted,it has been received as 1101011010. Detect the error using any one error detecting code
7	Explain about error detection and correction codes
	Part C
1	Explain the characteristics and implementation of the given digital logic families.(i) DTL(ii) RTL
2	Explain the basic working principles of following digital logic families. (i)TTL (ii)ECL (iii)CMOS
3	Explain the Hamming code with an example. State its advantages over parity codes

4	Design a TTL logic circuit for a 3 input NAND gate
	UNIT II COMBINATIONAL CIRCUITS
	PART-A
1	State & prove De-Morgan's theorem
2	Simplify the expression: X = (A'+B)(A+B+D)
3	Simplify Y = (A+B)(A'+C)
4	What is a prime implicant?
5	Define minterm and maxterm?
6	Minimize the function using K-map: F=$\sum$m(1,2,3,5,6,7)
7	Find the complement of F=x+yz.
8	Express x + yz as the sum of minterms.
9	Simplify: a) Y = AB'D + AB'D' b) Z = (A'+B)(A+B)
10	What are Universal Gates? Why are they called so?
11	Expressf(a,b,c) = a+b'c as sum of minterms
12	Give some of the major applications of multiplexers and decoders.
13	State the canonical forms of the Boolean function.
14	Given F=B'+A'B+A'C.Identify the redundant term using K-Map.
15	Apply DeMorgans theorems to simplify Y_1=(A+BC')', Y_2 = [A(B+C')D]
16	Draw a 1 to 2 demultiplexer circuit.
17	Draw a 2 to 1 multiplexer circuit.
	PART-B
1	Realize the circuit of a full adder in terms of two half adders.
2	Simplify the Boolean function using K-map F(w,x,y,z))=$\sum$ (0,4,6,8,9,10,12) which has the don'tcare conditions d(w,x,y,z)= $\sum$(2,13).
3	Implement the function F(p,q,r,s)=$\sum$(0,1,2,4,7,10,11,12) using decoder
4	Design a 4 bit Binary to gray code converter and implement using logic gates
5	Realize the circuit of a half subtractor with truth table
6	Realize the circuit of a 8:1 multiplexer
7	How does a encoder differ from a decoder and Demux differ from a mux?
	PART-C
1	Design 3 bit Gray Code to (i) binary converters using logic gates (ii) Excess-3 Code converter using NAND gates.
2	(i) Design BCD to Excess-3 code converter.
3	(ii)Implement the function F(x,y,z)=$\sum$(1,2,6,7) using Multiplexer
4	(i)Design a full adder circuit using NAND gates only.
5	Design a full subtractor and implement using logic gates.
6	Using K-map simplify the following function and implement the function using logic gates f(A,B,C) = $\prod$(0, 4, 6).
	UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS
	PART-A
1	What is the classification of sequential circuits?
2	Define Flip flop. What are the different types of flip-flop?
3	What is the operation of JK flip-flop? Why it is called a universal flip-flop?

4	What is the operation of D flip-flop and T flip-flop?
5	What is edge-triggered flip-flop?
6	What is a master-slave flip-flop?
7	Define rise time and fall time.
8	Define skew and clock skew
9	Define setup time.
10	Define hold time.
11	Draw the flip-flop excitation tables for RS FF.
12	Why gated D latch is called transparent latch?
13	What do you mean by present state and next state?
14	Give the comparison between combinational circuits and sequential circuits.
15	Compare synchronousand asynchronous sequential circuit.
16	What is the difference between level and edge triggering?
17	Draw truth table for D flip flop and JK flip flop?
18	How many flip flops are required to design mod 25 counter?
19	Differentiate between Mealy and Moore models.
	PART-B
1	Explain T-flip-flop with suitable internal structure
2	Draw a master-slave J-K flip-flop system. Explain its operation
3	Explain the various types of triggering with suitable diagrams. Compare their merits and demerits
4	Explain the concept of Race around condition in JK Flip flop and SR Flip Flop
5	Explain the conversion of T Flip Flop to D Flip flop
6	Write a note on 4 bit shift register with neat sketch
	PART-C
1	Design a BCD counter using JK flip-flops
2	Design an up-down counter using D-flip-flops to count 0, 3, 2, 6, 4, 0,.....
3	Design a 3-bit binary counter using T-flip flop
4	Design an asynchronous Modulo-8 Down counter using JK flipflops.
5	(ii)Explain the circuit of SR flipflpop and explain its operation
6	(i)Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flipflop for the design
	UNIT IV-ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES
	PART-A
1	Define secondary variables and excitation variables
2	What are races?
3	Define race conditions in asynchronous sequential circuit
4	Define non critical and critical race.
5	What is a dead lock condition
6	What are the different techniques used in state assignment?
7	What is hazard?
8	What is static 1 hazard and static 0 hazard?
9	What is dynamic hazard?
10	What is the cause for essential hazards?
11	Define merger graph.

12	Define state table
13	What are the steps for the design of asynchronous sequential circuit
14	Define primitive flow table
15	What are the types of asynchronous circuits?
16	Explain about state Assignment in Synchronous circuit and asynchronous circuit.
17	What is the difference between PROM AND EPROM
18	What is the difference between flow table and transition table?
19	Define PROM.
20	Give the classification of PLDs.
21	Define PLA.
	PART-B
1	Give the design Procedure for asynchronous sequential circuit
2	(I)Describe with diagram internal architecture of PLA (II)Design half adder circuit using PLA.
3	Give the classification of memories. Differentiate static and dynamic memories.
4	A certain memory stores 8 k x 16 bit words. How many data input lines, data output lines and address lines does it have? What is its capacity in bytes?
5	Realize the follwing the boolean function using PAL. $Y_1=\sum m(1,3,5,7)$ $Y_2=\sum(2,4)$
6	Realize the follwing the boolean function using PAL. $Y_1=\sum m(2,4,6,7)$ $Y_2=\sum(1,3)$
	PART-C
1	sketch the transition table and state table for an asynchronous sequential circuit described by the following Boolean expressions: $y_1=x_1x_2+x_1y_2+x_2y_1$, $y_1=x_2+x_2y_1y_2+x_1y_1$, $z=x_2+y_1$
2	Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.
3	Consider the following asynchronous sequential circuit and draw maps and transition table and state table.
	
4	Sketch the transition table and state table for an asynchronous sequential circuit described by the following Boolean expressions: $y_1=x_1x_2+x_1y_2+x_2y_1$, $y_1=x_2+x_2y_1y_2+x_1y_1$, $z=x_2+y_1$
5	Design a combinational circuit which accepts three bit number and outputs a binary number equal to the square of the input number using PROM.

6	Implement the boolean function using PLA: $F_1(A,B,C)=\sum(0,1,2,4)$ and $F_2(A,B,C)=\sum(0,5,6,7)$.
	UNIT V- VHDL
	PART-A
1	Write some of the Low Level Languages and High Level Languages?
2	What are the types of simulation?
3	what are the different modelling techniques used to describe a module?
4	What is static timing analysis?
5	Define gate level simulation.
6	What is the purpose of VHDL programming?
7	What is the need for VHDL?
8	What are sequential and concurrent statements?
9	What are the main components of a VHDL description?
10	What is entity?
11	Give the classification of data types supported by VHDL.
12	Give the syntax for VHDL entity declaration?
13	What is architecture?
14	List the internal details of an entity specified by architecture body.
15	Give the syntax for VHDL architecture declaration
16	What is the use of configuration declaration?
17	What is the need of package declaration?
18	What is subprogram?
19	List the different types of operators supported by VHDL?
20	The 'module' is the basic building block of VHDL. What are the different modeling techniques used to describe a module?
	PART-B
1	Briefly explain about the features of VHDL
2	Explain the digital system design flow sequence with the help of a flowchart.
3	Briefly discuss the use of Packages in VHDL
4	Write the VHDL code for D Flip Flop using behaviural modelling
5	Write the VHDL Code for D Flip Flop
6	Write the VHDL Code for XOR Gate using data flow modelling
7	Write the VHDL Code for Half Adder using Data flow modelling
8	Write the VHDL Code for Full Adder using Data Flow modelling
9	Write the VHDL Code for 4:1 Mux using Data flow modelling
10	Explain the various operators availble for VHDL
	PART C
1	Explain about the different types of architectural description. Write VHDL code for MUX using any two description type
2	Write a VHDL code for a 4-bit universal shift register
3	Write a VHDL program to implement SR latch and JK-flip flop using behavioral model.
4	Write aVHDL code that implements an 8:1 multiplexer
5	Write HDL for (i) four bit adder (ii) Mod 8 Counter
6	Write VHDL for four bit binary counter with parallel load and explain.
7	Explain test bench with suitable example.